UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/765,372	01/27/2004	Richard Westhoff	ASC-066	1594

51414 7590 05/05/2006

GOODWIN PROCTER LLP
PATENT ADMINISTRATOR
EXCHANGE PLACE
BOSTON, MA 02109-2881

EXAMINER	
MALSAWMA, LALRINFAMKIM HMAR	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/765,372	WESTHOFF ET AL.	
	Examiner	Art Unit	
	Lex Malsawma	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52 and 76-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *35* is/are allowed.

6)☒ Claim(s) *1-34,36-52 and 76-81* is/are rejected.

7)☒ Claim(s) *35* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The formal drawings (including the amendment to Figure 5) were received on 13 February 2006. These drawings are acceptable.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1, 4-9, 23-25, 37, 38 and 76-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schaake et al. (4,960,728; hereinafter "**Schaake**") in view of Nakamura et al. (US 2004/0060518 A1; hereinafter "**Nakamura**").

Regarding claims 1 and 4-9:

Schaake discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate (not shown, e.g., note Col. 2, lines 26-28);

forming a semiconductor layer 12 (Fig. 1) over a top surface of the substrate, the semiconductor layer including at least two elements (Te, Hg, Cd) that are distributed to define an initial compositional variation within the semiconductor layer (Col. 2, lines 21-45);

annealing the semiconductor layer to reduce the initial compositional variation (Fig. 2 and Col. 3, lines 33-39);

the initial compositional variation varies periodically within the semiconductor layer in a direction perpendicular to a semiconductor layer deposition direction (i.e., note elements 14 and 16 in Fig. 1);

the initial compositional variation defines a column within the semiconductor layer 12, the column having a width and a period (note the width and period of either "14" or "16");

the columnar period being less than approximately 2000 or 1000 nanometers (i.e., less than 20,000 or 10,000 angstroms, note Col. 2, lines 31-33, wherein element "14" has a thickness of about 1000-3000 angstroms and element "16" is a few hundred angstroms thick); and

the semiconductor layer is annealed at an annealing temperature and for a duration sufficient to diffuse at least one of the two elements (Cd or Hg, note Fig. 2) through a diffusion length at least equal to a quarter of the columnar period, i.e., Schaake discloses the annealing step homogenizes the semiconductor film 12, accordingly, the at least one element (Cd or/and Hg) would diffuse throughout the columnar period.

Schaake **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Schaake by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

Regarding claims 23 and 25:

Schaake discloses the top surface of the semiconductor layer 12 is planarized while the semiconductor layer is annealed (Col. 3, lines 43-45).

Regarding claim 24:

Schaake discloses (in Fig. 2) forming a layer 22 on the top surface of the semiconductor layer 12 prior to annealing, wherein the layer 22 provides a planarized top surface; accordingly, Schaake discloses the top surface of the semiconductor layer is planarized before the semiconductor layer is annealed.

Regarding claims 37 and 38:

Schaake discloses (in Fig. 1) the semiconductor layer 12 has an undulating surface 20 that is formed during deposition (Col. 2, lines 13-32).

Regarding claims 76-79:

Nakamura discloses (in section 0009) the source gases are injected into the reaction chamber from one of the sidewalls of the chamber; accordingly, the reactor is a horizontal flow deposition chamber and the reactor would be a single wafer reactor. Nakamura further discloses (in section 0010) when utilizing such a "horizontal flow" deposition chamber, the rotation of the

substrate essentially results in highest concentration of reactants disposed on the leading edges of the substrate; accordingly, Schaake modified by utilizing a horizontal flow deposition chamber would result in higher fraction of a first element of the semiconductor layer disposed in a leading edge of the substrate. With respect to claim 79, the column would essentially comprise a graded composition wherein the highest concentration would be disposed on the leading edges, as taught by Nakamura; therefore, the "graded" column could be readily described as "a graded column" comprising a high concentration of a first element (located at the leading edge of the substrate), the compositional variation (within the "graded" column) defines a second column within the semiconductor layer, and the second column comprises a low concentration of the first element. In other words, claim 79 is considered to contain limitations for a graded column that is formed when Schaake's method is performed using a horizontal flow deposition chamber (as taught by Nakamura).

5. Claims 1-3, 19-22 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bedell et al. (6,841,457 B2; hereinafter "**Bedell**") in view of **Nakamura** (US 2004/0060518 A1).

Regarding claims 1, 21 and 22:

Bedell discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate ("14/12/10" in Fig. 1A);

forming a semiconductor layer 16 over a top surface of the substrate (Fig. 1B), the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (Col. 6, lines 35-46); and

annealing the semiconductor layer to reduce the initial compositional variation (Col. 8, lines 13-23 and Figs. 1B-1D).

Bedell **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Bedell by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

Regarding claim 2:

Bedell discloses the substrate has a first lattice constant (i.e., the substrate comprises layer "14', which is single crystal silicon, e.g., note Col. 6, line 37), the semiconductor layer 16 has a second lattice constant (i.e., layer "16" is a SiGe alloy layer, e.g., not Col. 6, lines 35-39), and the first lattice constant differs from the second lattice constant, i.e., the lattice constant of single crystal silicon inherently differs from the lattice constant of a silicon-germanium layer.

Regarding claim 3:

Bedell discloses a first element (silicon) has a first concentration, x, a second element (germanium) has a second concentration, 1-x, and each of the first and second concentrations is at least 5%. Note in column 6 (lines 45-46), Bedell discloses the germanium concentration is preferably from about 10 to 35 percent, accordingly, the silicon concentration would be about 90 to 65 percent.

Regarding claims 19 and 20:

Bedell discloses the semiconductor layer is annealed at an annealing temperature below a melting point of the semiconductor layer (Col. 9, lines 5-10), wherein the annealing temperature may be as low as 900 °C (Col. 8, lines 42-45).

Regarding claim 42:

Bedell discloses forming a protective layer 18 over the semiconductor layer 16 prior to annealing the semiconductor layer (Col. 7, lines 1-4).

6. Claims 1 and 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamane et al. (4,914,488; hereinafter "**Yamane**") in view of **Nakamura** (US 2004/0060518 A1).

Regarding claims 1 and 10-15:

Yamane discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 1 (Fig. 5A and Col. 8, line 45);

forming a semiconductor layer 5/6 over a top surface of the substrate (Fig. 5B), the semiconductor layer including at least two elements (Al, Ga, As, or Si), the elements being distributed to define an initial compositional variation within the semiconductor layer (Col. 8, lines 50-54, 60-68; and Col. 9, lines 1-28);

the initial compositional variation varies in a direction parallel to a semiconductor layer deposition direction and defines a superlattice having a periodicity, wherein the periodicity is less than approximately 10 nanometers (e.g., 2.5 nm, note Col. 9, lines 23-25); and

annealing the semiconductor layer to reduce the initial compositional variation, wherein the annealing is performed at a temperature and for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice (i.e., the annealing causes mutual diffusion to transform the superlattice into a continuous layer, see Col. 5, lines 57-61 and Col. 7, lines 15-28).

Yamane **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Yamane by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

7. Claims 1, 16-18 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christiansen et al. (6,515,335 B1; hereinafter "**Christiansen**") in view of **Nakamura** (US 2004/0060518 A1).

Regarding claims 1 and 16-18:

Christiansen discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate ("10/20/30/40" in Fig. 1A);

forming a semiconductor layer 50/60 over a top surface of the substrate (Fig. 1A), the semiconductor layer including at least two elements (silicon and germanium), the elements being

distributed to define an initial compositional variation within the semiconductor layer (Col. 5, lines 18-30 and Col. 6, lines 5-15);

annealing the semiconductor layer to reduce the initial compositional variation, thereby obtaining a homogeneous, uniform composition layer 70 (Col. 6, lines 42-46; the paragraph bridging Cols. 6-7; and Col. 2, lines 53-60);

the annealing temperature (800-1250 °C, note Col. 6, lines 50-52) being greater than the deposition temperature (e.g., 550-700 °C, note Col. 5, lines 28-29).

Christiansen **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Christiansen by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

Regarding claim 41:

Christiansen discloses an optional graded layer 65 may be incorporated (Col. 8, lines 1-7), wherein the graded layer 65 is formed below the semiconductor layer 70 (Fig. 3) and is acquired by the annealing process, which formed the relaxed, homogenous/uniform composition layer 70; accordingly, layer "65' is a relaxed graded layer formed over the substrate.

8. Claims 1, 22, 23, 31, 32, 34 and 42-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Notsu et al. (US 2002/0146892 A1; hereinafter "**Notsu**") in view of **Nakamura** (US 2004/0060518 A1).

Regarding claims 1, 22, 23, 31, 32, 34 and 42-44:

Notsu discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 11/12 (Fig. 1B);

forming a semiconductor layer 13/14 over a top surface of the substrate (Fig. 1B), the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (paragraphs 0101-0102);

forming a protective layer 15/21 (silicon dioxide, note Fig. 1B and paragraph 0102) over the semiconductor layer 13/14 prior to annealing the semiconductor layer, wherein the protective layer is substantially inert with respect to the semiconductor layer (note the first two sentences in paragraph 0103);

bonding a top surface of the semiconductor layer 13/14 to a wafer 31 (Fig. 1C, note that although the top surface of the semiconductor layer 13/14 may not be in direct physical contact with the wafer, the top surface is nevertheless bonded to the wafer);

removing at least a portion of the substrate 11/12, wherein at least a portion of the semiconductor layer 13/14 remains bonded to the wafer after the portion of the substrate is removed;

planarizing the top surface of the semiconductor layer (note Figs. 1D-1E and in paragraph 0106, Notsu discloses polishing the remaining portions 12' such that a the top surface of the semiconductor layer is exposed, wherein the polishing would also remove a portion of the semiconductor layer, thereby providing a planarized top surface);

annealing the semiconductor layer to reduce the initial compositional variation, i.e., a layer 14" is formed from layer 13/14 by the annealing process such that the germanium concentration with the layer 14" becomes almost uniform (note paragraph 0113); and

forming a second layer 41 (Fig. 2B) over the semiconductor layer 14" subsequent to planarizing the top surface of the semiconductor layer, wherein the second layer 41 comprises a material having a lattice constant substantially different from a lattice constant of the semiconductor layer (paragraph 0114).

Notsu **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Notsu by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

9. Claims 1, 22 and 26-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Malik et al. (US 2004/006744 A1; hereinafter "**Malik**") in view of **Hsu et al.** (US 2002/0168802 A1) and **Nakamura** (US 2004/0060518 A1).

Regarding claims 1, 22, 26 and 27:

Malik discloses (in Fig. 1 and paragraphs 0013-0016) a method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements (silicon and germanium), the elements being distributed to define an initial compositional variation within the semiconductor layer (i.e., the initial compositional variation provides a strained film);

annealing the semiconductor layer to reduce the initial compositional variation, thereby providing a relaxed SiGe film;

planarizing a top surface of the SiGe film by chemical-mechanical polishing (CMP).

Although Malik does not specifically recite that the annealing step reduces the initial compositional variation, the annealing process performed to relax the SiGe film will reduce the initial compositional variation in at least some portions of the SiGe film in order to obtain the relaxed SiGe film. **Hsu et al.** (US 2002/0168802 A1) **is cited only** to show that an annealing process applied to a SiGe film will result in reduction of an initial compositional variation of the SiGe film, i.e., Hsu et al. discloses (in paragraph 0008) the annealing/heat-treatment diffuses Ge from/within the SiGe film. Accordingly Malik's annealing process performed to relax the SiGe film will diffuse Ge such that the initial compositional variation, at least with respect to Ge, in at least some portions will be reduced.

Malik **lacks** rotating the substrate during the formation of the semiconductor layer. Nakamura **teaches** (in section 0009) it was well known in the art to rotate a substrate during deposition in order to obtain a more uniform growth. It would have been obvious to one of ordinary skill in the art to modify Malik by rotating the substrate because Nakamura teaches rotating a substrate during deposition provides a more uniform growth, e.g., more uniform growth with respect to the thickness of the grown layer.

Regarding claims 28 and 29:

Malik discloses the CMP comprises a first and second step and semiconductor layer is annealed between the first and the second CMP steps, wherein the first step is considered to be "step 110" shown in Fig. 1 and the second step is considered to be "step 130" shown in Fig. 1. In other words, the current claims do not require two separate CMP processes, but rather, they only requires a CMP process comprising a first and second step, wherein no manufacturing process steps could be (or should be) excluded from being interpreted as either the first step or the second step, so long as one of the steps is a CMP process. *Specifically regarding claim 29:* Malik discloses (in Fig. 1) the "cycle" may be repeated if necessary, i.e., in a case wherein the "cycle" is repeated, the CMP comprises a first and second step and the semiconductor layer is annealed before the first CMP step, wherein the first CMP step would be "step 130" and the second step would be "step 110".

Regarding claim 30:

Malik discloses the planarization step comprises a high temperature step (i.e., an annealing step "110" in Fig. 1) that would anneal the semiconductor layer. In other words, Malik discloses the planarization comprises a CMP step, which is preceded by an annealing step; accordingly, Malik discloses a planarization comprising a high-temperature step and a CMP step, wherein the semiconductor layer is annealed during the high-temperature planarization step.

10. Claims 23, 32, 33 and 36-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Yamane** (in view of **Nakamura**) as applied to claim 1 above, and further in view of **Ohori** (5,844,260).

Regarding claims 23, 32, 33 and 36:

Yamane (in view of Nakamura) further discloses forming a second layer 6/11/7 (Yamane, Fig. 9) having a lattice constant substantially equal to a lattice constant of the semiconductor layer 5 (Figs. 5A, 9), wherein the second layer 6/11/7 comprises (i) a lower portion having a superlattice 6 and (ii) an upper portion 11/7 disposed over the lower portion 6, the upper portion being substantially free of a superlattice in at least the open region where gate electrode 9 is formed. Yamane (in view of Nakamura) **lacks** planarizing a top surface of the semiconductor layer or planarizing the top surface prior to forming the second layer. Ohori **teaches** that a structure similar to that disclosed by Yamane would comprise an undulated surface (Col. 8, lines 24-32) and the effects of the undulated surfaces can be diminished or eliminated by planarizing/polishing the undulated surface prior to forming a subsequent layer (Figs. 7A-7C; Col. 3, lines 39-42; and Col. 11, lines 7-24). It would have been obvious to one of ordinary skill in the art to modify Yamane (in view of Nakamura) by planarizing the semiconductor layer prior to forming the second layer because Ohori teaches that planarizing the undulated surface of the superlattice layer(s) provides a flat surface for subsequent layer, thereby diminishing problems caused by the undulated surface.

Regarding claims 37-40:

Yamane (in view of Nakamura) **lacks** the semiconductor layer having an undulating surface. Ohori **teaches** that a superlattice structure, similar to that disclosed by Yamane, would typically have an undulating surface (Col. 8, lines 24-32) that is formed during deposition, and the undulating surface essentially results from an undulating substrate surface upon which the superlattice structure is formed (e.g., note the paragraph bridging Cols. 5-6); and the undulating

surface could have an amplitude exceeding 30 microns (Col. 8, line 31). Given Ohori, one of ordinary skill in the art could have easily modified Yamane (in view of Nakamura) by specifying that the semiconductor layer has an undulating surface because Ohori shows/teaches that a superlattice structure, similar to that in Yamane, would likely have such a surface. Furthermore, since Yamane discloses a superlattice having a periodicity of about 2.5 nm (note Col. 9, lines 23-25) and Ohori teaches that the amplitude of the undulating surface could be 30 microns (or more), the periodicity of the superlattice would obviously be less than the amplitude of the undulating surface.

11. Claims 45-49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ohori** (5,844,260) in view of Gay et al. (5,218,417; hereinafter "**Gay**").

Regarding claim 45:

Ohori discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 51 (Fig 7C);

selecting a first plurality of parameters suitable for forming a semiconductor layer (53, 55, 56, 57 and/or 58, i.e., the semiconductor layer would be any of these layer or any combination of these layers) over a top surface of the substrate 51, the semiconductor layer including at least two elements (Ga, As), the elements being distributed to define a compositional variation within the semiconductor layer;

forming the semiconductor layer having a haze (i.e., note the undulation shown on layer 53, which is a portion of the semiconductor layer (53, 55, 56 or 57), wherein the undulation could be referred to as a haze or at very least, the undulation produces haze); and

planarizing the semiconductor layer to remove the haze (note Col. 11, lines 10-14 and lines 39-46. It is noted that even if a combination of all layers (53, 55, 56 57, 58) are considered to be the semiconductor layer, the "semiconductor layer (53, 55, 56, 57, 58) is planarized to remove the haze, since the result after forming all the layers is a substantially haze free surface, e.g., note Col. 11, lines 44-49).

Ohori is silent with respect to the roughness wavelength of the haze; accordingly Ohori **lacks** the haze comprising a fine-scale roughness wavelength of < 1micrometer.

Gay **teaches** that "haze" is conventionally defined as the ratio of the diffuse/scattered component of transmitted light to the total amount of light transmitted by a thin film for the wavelengths of light to which a photodetector is sensitive (Col. 1, lines 15-20), and Gay discloses haze measurements performed utilizing wavelengths of 500 and/or 800 nm (e.g., note abstract; Col. 7, lines 34-36; and Col. 8, lines 63-68), i.e., the haze measured by Gay would have a roughness wavelength of less than 1 micrometer because wavelengths of 0.5 and 0.8 micrometers are utilized. Since Ohori is silent with respect to the roughness wavelength of haze, it would have been obvious to one of ordinary skill in the art to determine the haze in Ohori's semiconductor layer by utilizing any means known in the art; accordingly, it would have been obvious to one of ordinary skill in the art to incorporate Gay's measuring system to determine haze at a fine-scale roughness wavelength of less than 1 micrometers.

Regarding claim 46:

Ohori discloses the semiconductor layer (53, 55, 56, 57, 58) comprises a lower portion (55, 56, 57) including a superlattice and forming an upper portion over the lower portion, the upper portion (58) being substantially free of a superlattice (e.g., note Fig. 1, wherein the

superlattice region is "region 13" and the upper region "14" is substantially free of a superlattice).

Regarding claim 47:

Ohori discloses, in a first embodiment, the first plurality of parameters comprises at least temperature (note Col. 5, lines 60-62).

Regarding claim 48:

Ohori discloses the "haze" is removed by polishing layer 53 to a mirror-finish (Col. 11, lines 10-14), and after the polishing of layer "53", subsequent layers "55-57" are grown without haze (i.e., without cross-hatching, note Col. 11, lines 39-46). In order for the subsequent layers "55-57" to be grown without "haze", it is clear that the semiconductor layer must be cleaned after planarizing, especially because the polishing step would leave loose particles, slurry, etc. on the surface of the polished layer.

Regarding claims 49 and 52:

Initially, with respect to this claim, the semiconductor layer would be layer 53 (only). Ohori discloses selecting a second plurality of parameters suitable for forming a substantially haze-free re-growth layer (55, 56,57 and 58) over the semiconductor layer 53, the semiconductor layer 53 including at least two elements (Ga, As), the elements being distributed to define a compositional variation within the semiconductor layer (note that a process for forming the haze-free re-growth layer will require selecting a plurality of process parameters, e.g., parameters such as temperature, layer thickness, element concentrations, etc.); and

forming the substantially haze-free re-growth layer (55, 56, 57, 58), wherein the re-growth layer comprises forming a lower portion (55, 56) including a superlattice and forming an

upper portion (58) over the lower portion, the upper portion being substantially free of a superlattice (e.g., note Fig. 1, wherein the superlattice region is "region 13" and the upper region "14" is substantially free of a superlattice).

12. Claims 45 and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fitzgerald** (6,107,653) in view of **Gay** (5,218,417).

Regarding claims 45 and 49-51:

Fitzgerald discloses a method for forming a semiconductor structure, the method comprising:

providing a substrate 302 (Fig. 3);

selecting a first plurality of parameters suitable for forming a semiconductor layer 304 (Fig. 3) over a top surface of the substrate, the semiconductor layer including at least two elements (Si, Ge), the elements being distributed to define a compositional variation within the semiconductor layer;

forming the semiconductor layer having a haze (NOTE: Although Fitzgerald is silent with respect to the term, "haze", it is clear that the semiconductor layer will have a "haze" because a CMP step is performed to planarize the surface for the semiconductor layer 304, i.e., "surface unevenness" produces "haze"; accordingly, the semiconductor layer 304 has a haze because it has an uneven surface that requires planarization using a CMP step);

planarizing the semiconductor layer 304 utilizing a CMP process (Fig. 3 and Col. 54-62), wherein the planarizing step will remove the haze because the surface unevenness will be removed by the CMP process;

selecting a second plurality of parameters suitable for forming a substantially haze-free re-growth layer 306/308 over the semiconductor layer 304, the semiconductor layer 304 including at least two elements, the elements being distributed to define a compositional variation within the semiconductor layer;

forming the substantially haze-free re-growth layer (NOTE: Although Fitzgerald is silent with respect whether the re-growth layer 306/308 has haze or is haze-free, it is clear from the text in Col. 7, lines 6-20, that the re-growth layer should be haze-free because Fitzgerald specifies that a plurality of CMP steps should be incorporated if necessary, wherein at least one CMP step should be performed to planarize the re-growth layer; accordingly, Fitzgerald forms a substantially haze-free re-growth layer);

wherein the first plurality of parameters comprises a first temperature (750 °C, note Col. 3, lines 47-48), the second plurality of parameters comprises a second temperature (550 °C, note Col. 4, line 1 and/or Col. 4, lines 47-49), the first temperature being higher than the second temperature; and

wherein the first plurality of parameters comprises a first growth rate (e.g., a growth rate of germanium within the silicon-germanium layer, note Col. 4, lines 35-38), the second plurality of parameters comprises a second growth rate (e.g., a growth rate of silicon within the silicon-germanium layer 306/308), the first growth rate (of Ge) is higher than the second growth rate (Si) because the germanium growth rate increases as the silicon growth rate decreases.

Fitzgerald is silent with respect to the degree of surface roughness after the planarizing step, accordingly, Fitzgerald **lacks** the haze comprising a fine-scale roughness wavelength of < 1 micron.

Gay **teaches** that "haze" is conventionally defined as the ratio of the diffuse/scattered component of transmitted light to the total amount of light transmitted by a thin film for the wavelengths of light to which a photodetector is sensitive (Col. 1, lines 15-20), and Gay discloses haze measurements performed utilizing wavelengths of 500 and/or 800 nm (e.g., note abstract; Col. 7, lines 34-36; and Col. 8, lines 63-68), i.e., the haze measured by Gay would have a roughness wavelength of less than 1 micrometer because wavelengths of 0.5 and 0.8 micrometers are utilized. Since Fitzgerald is silent with respect to the roughness wavelength of haze, it would have been obvious to one of ordinary skill in the art to determine the haze in Fitzgerald's semiconductor layer by utilizing any means known in the art; accordingly, it would have been obvious to one of ordinary skill in the art to incorporate Gay's measuring system to determine haze at a fine-scale roughness wavelength of less than 1 micrometers.

13. Claims 80 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Ohori** (in view of **Gay**) as applied to claim 45 above, and further in view of Yonehara et al. (US 2003/0159644 A1; hereinafter "**Yonehara**").

Regarding claims 80-81:

Ohori (in view of Gay) **lacks** the top surface of the semiconductor layer specifically having a roughness root-mean-square (RMS) of less than 5 angstroms (or less than 1 angstrom) in a scan area of 40μm x 40μm. However, note that Ohori discloses (in Col. 11, lines 10-14) the top surface of the semiconductor layer is polished to a mirror-finish within a precision of less than 1μm. Since Ohori does not specify exactly how much less than 1μm the surface roughness

would be, one of ordinary skill in the art could have polished the surface to any roughness (RMS) under 1μm.

Yonehara **teaches** than planarizing processes (such as a CMP process, similar to Ohori's planarizing process) known in the art are readily capable of providing surface roughness RMS of less than 5 angstroms (0.5nm) in a scan area of 50μm x 50μm (note sections 0361, 0093 and 0094).

Given that planarizing processes are generally performed to provide as smooth a surface as possible and that Ohori does not specify how much less than 1μm the surface roughness should be, it would have been obvious to one of ordinary skill in the art to polish Ohori's semiconductor layer to have a roughness of less than 5 angstroms in a scan area of 50μm x 50μm because Yonehara teaches that such a roughness is attainable by a planarizing process similar to that disclosed by Ohori and further because one practicing Ohori's process would desire a surface that is as smooth as possible, especially since Ohori specifies the polished surface should have a mirror-finish.

With respect to claim 81, although Ohori (in view of Gay and Yonehara) does not specifically disclose a roughness RMS of less than 1 angstrom, this claim is deemed obvious over the cited references because (i) the cited references disclose the general conditions of the claimed invention and (ii) a roughness RMS of less than 1 angstrom is considered to be an optimum or workable range for some specific design requirement. In other words, given the general conditions disclosed by the cited references, finding an optimum or workable range (for roughness-RMS) for some particular design requirement would have involved only routine skill in the art. Note that it has been held that where the general conditions of a claim are disclosed in

the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller,* 105 USPQ 233.

Allowable Subject Matter

14. Claim 35 is allowable for reasons stated in the prior Office action.

Remarks

15. Applicant's remarks/arguments have been carefully reviewed and considered, but they are not persuasive for the following reasons.

With respect to Schaake and Yamane, applicant's remarks are moot in view of the new ground of rejection.

With respect to Bedell, the applicant asserts that Bedell's anneal apparently causes Ge atoms to merely be redistributed within the Si_xGe_{1-x} layer and Si layer, and Bedell appears to disclose redistribution of Ge in two layers without teaching or suggesting reduction of an initial compositional variation within a layer. If Bedell discloses "redistribution" of Ge in two layers, wherein one of the two layers was a Si layer, then is apparently follows that the initial compositional variation within the Si_xGe_{1-x} (as originally formed) will be reduced, i.e., an initial compositional variation with respect to Ge in the "original" Si_xGe_{1-x}, prior to anneal, will be reduced because some of the Ge atoms "redistribute" into the Si layer as suggested by the applicant. With respect to rotating the substrate, the remarks are moot in view of the new ground of rejection.

With respect to Christiansen and Notsu, applicant's remark are not persuasive for reasons similar to those provided above with respect to applicant's remarks/arguments directed to Bedell.

With respect to Malik and Hsu, the applicant asserts that Hsu is silent about reducing initial compositional variations, since Hsu merely employs an anneal to form a relaxed SiGe film. In the referenced text of Hsu (i.e., section 0008), Hsu clearly discloses, "This heat treatment diffuses the Ge to convert the top silicon film into relaxed $Si_{1-x}Ge_x$..."; therefore, it is clear that some of the Ge atoms within the initial SiGe layer diffuse into the top silicon film; accordingly, the initial compositional variation in the initial SiGe layer is reduced. Since Malik anneals a SiGe layer formed directly on a Si wafer, it is clear from Hsu's teaching that some of the Ge atoms within Malik's SiGe layer would diffuse into the silicon wafer. Therefore, applicant's remarks are not persuasive. With respect to rotating the substrate, applicant's remarks are moot in view of the new ground of rejection.

With respect to claims 45-52, Ohori and Fitzgerald, applicant's remarks are moot in view of the new grounds of rejections.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lex Malsawma whose telephone number is 571-272-1903. The examiner can normally be reached on Mon. - Thur. (4-12 hours between 5:30AM and 10 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lex Malsawma

April 28, 2006

Brook Kebede

BROOK KEBEDE
PRIMARY EXAMINER